Patent Claims:

1. An electrical device (200) for efficient and flexible control of memory access, said device (200) being

- connected to at least one memory accessing unit (202), and
- connected to a memory (100) comprising at least one physical memory module (203),

said device (200) comprising

- at least two access channel circuits (300), where at least one access channel circuit (300) is connected to said least one memory accessing unit (202) via at least one system bus (304; 308) and to said at least one physical memory module (203), said at least one access channel circuit (300) providing memory access for said at least one memory accessing unit (202) to at least a part of said memory (100).

2. An electrical device (200) according to claim 1, characterized in that said at least two access channel circuits (300) each provides memory access for at least one memory accessing unit (202) to at least a part of the memory (100) thereby allowing memory accessing units (202) connected to different access channel circuits (300) independent and simultaneous/parallel access to different parts of the memory (100).

3. An electrical device (200) according to claims 1 - 2, characterized in that said device (200) comprises

- a control and configure circuit (201) dynamically controlling said at least two access channel circuits (300), said control and configure circuit (201) allowing for simple addition of further access channel circuits (300) during implementation.

4. An electrical device (200) according to claims 1 - 3, characterized in that said device comprises at least two access channel circuits (300) each being connected via a single system bus (304, 308) to a single memory accessing unit (202) and each being connected (210) to receive information/data from at least a part of said memory (100).

5. An electrical device (200) according to claims 1 – 4, characterized in that said device (200) comprises one access channel circuit (300) connected via a single system bus (304, 308) to at least two memory accessing units (202), said one access channel circuit (300) being connected (210) to receive data/information from and/or transmit data/information to at least a part of said memory (100).

6. An electrical device according to claims 1 – 5, characterized in that an access channel circuit (300) further comprises an automatic data transfer engine (301) for transferring data/information from a first physical memory module (203) of the memory (100) to a second physical memory module (203) of the memory (100) prior to a memory accessing device (202) retrieving said data/information.

7. An electrical device according to claim 6, characterized in that automatic data transfer engines (301) of a plurality of access channel circuits (300) are connected to form a chain of automatic data transfer engines where each data transfer engine (301) is responsible for transferring a different part of said data/information.

8. An electrical device according to claims 3 – 7, characterized in that said at least one access channel circuits (300) comprises at least one special purpose register and is connected (307) to said control and configure circuit (201), where said control and configure circuit (201) is adapted to modify a content of said at least one special purpose register thereby allowing for reconfiguration of individual access channel circuits (300) without affecting other access channels (300) during operation.

9. An electrical device according to claim 8, characterized in that said reconfiguration comprises configuring a mode of functionality and/or at least one access region of said memory (100).

10. An electrical device according to claims 1 – 9, characterized in that said device (200) comprises one access channel circuit (300) for each connected memory accessing unit (202) and in that each access channel

circuit (300) is connected with each memory module (203) of said memory (100).

11. An electrical device according to claims 1 - 10, c h a r a c t e r i z e d in that an access channel circuit (300) comprises

- a memory access controller (301) adapted to monitor an incoming system bus (304), connected to a memory accessing device (202), and an outgoing system bus (308) connected to a memory accessing device (202) for a first identifier representing a given memory bus (209) to be connected, the memory access controller (301) providing a first control signal/code, based on said first identifier, representing said given memory bus (209) and to where said given memory bus (209) is to be connected,
- a source and destination selector (303) for enabling access to a memory bus (209), connected to a memory module (203) of said memory (100), from said incoming system bus (304) or said memory access controller (301) dependent on said first control signal/code received from said memory access controller (301), and
- a memory module selector (302) for selecting which memory module (203) is to be connected to the outgoing system bus (308), connected to said memory accessing device (202), during a given read access of a specific memory module (203) dependent on a second unique identifier.

12. A method of efficient and flexible control of memory access between at least one memory accessing unit (202) and a memory (100) comprising at least one physical memory module (203), the method comprising the step of:

- providing, by at least one of at least two access channel circuits (300), memory access for said at least one memory accessing unit (202) to at least a part of said memory (100), where said at least one access channel circuit (300) is connected to said least one memory accessing unit (202) via at least one system bus (304; 308) and to said at least one physical memory module (203).

13. A method according to claim 12, c h a r a c t e r i z e d in that said method comprises the step of:

- providing simultaneous memory access for said at least two memory accessing units (202) to at least a part of the memory (100) via said at least two access channel circuits (300), each access channel providing independent access to different parts of the memory (100), thereby allowing memory accessing units (202) connected to different access channel circuits (300) parallel access to different parts of the memory (100).

14. A method according to claims 12 - 13, characterized in that said method further comprises the step of:

- dynamically controlling said at least two access channel circuits (300) by a control and configure circuit (201), said control and configure circuit (201) allowing for simple addition of further access channel circuits (300) during implementation.

15. A method according to claims 12 - 14, characterized in that said method further comprises the step of:

- providing memory access to a single memory accessing unit (202) from at least a part of said memory (100) by at least two access channel circuits (300) each being connected via a single system bus (304, 308) to the single memory accessing unit (202) and each being connected (210) to receive information/data from at least a part of said memory (100).

16. A method according to claims 12 – 15, characterized in that said method comprises the step of:

- providing memory access to at least two memory accessing units (202) from at least a part of said memory (100) by a single access channel circuit (300) connected via a single system bus (304, 308) to said at least two memory accessing units (202), said single access channel circuit (300) being connected (210) to receive data/information from and/or transmit data/information to at least a part of said memory (100).

17. A method according to claims 12 – 16, characterized in that said method further comprises the step of:

- providing automatic data transfer of data/information by an access channel circuit (300) comprising an automatic data transfer engine (301) for transferring data/information from a first physical memory module (203) of the memory (100) to a second physical memory module (203) of the memory (100) prior to a memory accessing device (202) retrieving said data/information.

18. A method according to claim 17, c h a r a c t e r i z e d in that said method comprises the step of:

- providing automatic data transfer of data/information where a plurality of automatic data transfer engines (301) of a plurality of access channel circuits (300) are connected to form a chain of automatic data transfer engines and
- where each data transfer engine (301) is responsible for transferring a different part of said data/information.

19. A method according to claims 14 – 18, c h a r a c t e r i z e d in that said method comprises the step of:

- modifying, by said control and configure circuit (201), a content of at least one special-purpose register, comprised by at least one access channel circuit (300) connected (307) to said control and configure circuit (201), thereby allowing for reconfiguration of individual access channel circuits (300) without affecting other access channels (300) during operation.

20. A method according to claim 19, c h a r a c t e r i z e d in that said reconfiguration comprises configuring a mode of functionality and/or at least one access region of said memory (100).

21. A method according to claims 12 – 20, c h a r a c t e r i z e d in that memory access is provided by one access channel circuit (300) for each connected memory accessing unit (202) where each access channel circuit (300) is connected with each memory module (203) of said memory (100).

22. A method according to claims 12 - 21, c h a r a c t e r i z e d in that said method further comprises the steps of:

- monitoring, by a memory access controller (301) comprised by an access channel circuit (300), an incoming system bus (304), connected to a memory accessing device (202), and an outgoing system bus (308) connected to a memory accessing device (202) for a first identifier representing a given memory bus (209) to be connected,
- providing, by the memory access controller (301), a first control signal/code, based on said first identifier, representing said given memory bus (209) and to where said given memory bus (209) is to be connected,
- enabling access, by a source and destination selector (303), to a memory bus (209), connected to a memory module (203) of said memory (100), from said incoming system bus (304) or said memory access controller (301) dependent on said first control signal/code received from said memory access controller (301), and
- selecting, by a memory module selector (302), which memory module (203) is to be connected to the outgoing system bus (308), connected to said memory accessing device (202), during a given read access of a specific memory module (203) dependent on a second unique identifier.

23. Use of an electrical device according to claims 1 - 11, characterized in that said electrical device (200) is used in a mobile communications terminal (501).

24. Use of a method according to claims 12 - 22, characterized in that said method is used in a mobile communications terminal (501).

25. A computer-readable medium having stored thereon instructions for causing a processing unit to execute the method according to any one of claims 12 - 22.